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10/019,437	12/31/2001	Yasuyuki Doi	60188-124	4255

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EXAMINER

NELSON, ALECIA DIANE

ART UNIT

PAPER NUMBER

2675

DATE MAILED: 10/06/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

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# Office Action Summary

Application No.

10/019,437

Applicant(s)

DOI ET AL.

Examiner

Alecia D. Nelson

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-14 is/are allowed.
- 6) ☐ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) 6-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Priority*

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/16/1999. It is noted, however, that applicant has not filed a certified copy in the current application as required by 35 U.S.C. 119(b).

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on 12/31/01, has been considered by the examiner as indicated on PTO Form-1449.
3. The information disclosure statement filed fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 2-8** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claims 2 and 3 the applicant recites "the same

number", referring to the branch reference voltage wires and the buffers, however it is not defined to what these component have the same number of what other component(s) and what that number is defined as. **Claims 4-8** are rejected as being dependent on a rejected base claim.

6. Claim 6 recites the limitation "the other terminal" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 9 recites the limitation "the other terminal" in line 11 of the claim. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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10. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (U.S. Patent No. 6,221,849) in view of Applicant's admittance of prior art.

With reference to **claim 1**, Sasaki et al. teaches a liquid crystal driving circuit in which a plurality of source driver circuit devices (23) for driving a liquid crystal element are arranged on a liquid crystal panel (22) (see column 3, lines 50-65), the liquid crystal driving circuit comprising a reference voltage production circuit (interface unit, 25) for producing a plurality of signals, including power voltage, pixel data, clock data and other control signals, for driving the liquid crystal element (see column 4, lines 3-7);

Sasaki et al. fails to specifically teach a plurality of reference voltage wires for supplying the plurality of reference voltages to the source driver circuit devices, however does teach that the interface unit sends power voltage and control signals to the line driver (24), and power voltage, pixel data, clock data, and control signals to the signal driver (23). Figure 2 illustrates a bus connection from the interface 25 to the drivers 23 and 24. Therefore it is obvious that there are a plurality of wires for supplying signals to the driver circuits. Sasaki et al. also fails to specifically teach that the reference voltage wires extend through an area on the liquid crystal panel and an area on each of the source drivers circuit devices. However the disclosed invention teaches that the drivers ICs (1) are formed on the corresponding driver substrate by the COG mounting technique. Further it is taught that the inter-module wirings (10) connect the driver ICs in cascade, so as to transmit the data from interface (25) to each of the driver ICs.

Therefore it would be obvious that the wires extend through an area on the liquid crystal

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panel being that the driver ICs are COG mounted to the substrate and there are wires leading from the interface (25) to the drivers (23, 24).

Moreover, the applicant's admittance of prior art teaches with reference to the reference voltage wires, the usage of voltage production/control circuit (120) having reference voltage wires (131).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the control circuit and wires, as taught by the admitted prior art, in a system similar to that which is taught by Sasaki et al., which suggest such signals being transmitted by wires to thereby generate control signals that are transmitted through reference voltage wires to the driver circuitry which uses a COG technique for mounting the drivers to the LC substrate in order to prevent an increase in the dimensions of the frame region and in the manufacturing cost.

With reference to **claim 2**, Sasaki et al. teaches that the driving circuit (1) includes a plurality of in-chip reference voltage wires (10) extending from one end to the other end of the source driver circuit device for supplying a plurality of reference voltage different from one another (see Figure 3). Sasaki et al. also teaches that various power voltages are input to the driver (1) via the power input (11) and the supplied to circuit components such as the buffer amplifiers (4, 8), and other circuitry and are output to the next driver IC (see column 7, lines 6-15).

Sasaki et al. fails to teach branch reference voltage wires branching from the plurality of in-chip reference voltage wires, and selector for selecting a voltage for driving the LC element supplied from the buffer.

The admitted prior art teaches the usage of branch reference voltage wires (131) branching off from the plurality of in-chip reference voltage wires, a selection circuit (134) for selecting, a voltage for driving the liquid crystal element.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the usage of the branch reference voltage wires and a selection circuit as disclosed by the admitted prior art in the driver circuits similar to that, which is taught by Sasaki et al. to thereby reduce the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes without increasing the dimensions of the frame region.

With reference to **claim 3**, Sasaki et al. teaches a semiconductor integrated circuit device provided in a liquid crystal module and carrying thereon a source driver circuit (23) for driving a liquid crystal element wherein the source driver includes, includes a plurality of in-chip reference voltage wires (10) extending from one end to the other end of the source driver circuit device for supplying a plurality of reference voltage different from one another (see Figure 3). Sasaki et al. also teaches that various power voltages are input to the driver (1) via the power input (11) and the supplied to circuit components such as the buffer amplifiers (4, 8), and other circuitry and are output to the next driver IC (see column 7, lines 6-15).

Sasaki et al. fails to teach branch reference voltage wires branching from the plurality of in-chip reference voltage wires, and selector for selecting a voltage for driving the LC element supplied from the buffer.

The admitted prior art teaches the usage of branch reference voltage wires (131) branching off from the plurality of in-chip reference voltage wires, a selection circuit (134) for selecting, a voltage for driving the liquid crystal element.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the usage of the branch reference voltage wires and a selection circuit as disclosed by the admitted prior art in the driver circuits similar to that, which is taught by Sasaki et al. to thereby reduce the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes without increasing the dimensions of the frame region.

With reference to **claim 4**, Sasaki et al. fails to teach that the semiconductor integrated circuit device further includes a subdivided voltage production circuit (132), wherein the selection circuit selects one of the subdivided voltages.

The admitted prior art teaches these limitations of claim 4 including the subdivided voltage production circuit (132) and the selection circuit (134) (see pages 5-6).

Therefore it would have been obvious to one having ordinary skill in the art to allow the device of Sasaki et al. to include the subdivided voltage production circuit and the selection circuit as taught by admitted prior art in order to generate voltage signals



for controlling the brightness of light passing through the liquid crystal element when driving the liquid crystal display panel thereby producing higher resolution for larger screen sizes without increasing the dimensions of the frame region.

11. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. and admitted prior art as applied to claim 1 above, and further in view of JP Patent No. 3-165118, hereinafter 3-165118).

Sasaki et al. and the admitted prior art teaches all that is required as explained above with reference to **claim 1**, however fails to teach that the that the buffer has an offset canceling function.

3-165118 teaches the usage of two switched capacitor circuits for a complementary operation, which are capable of canceling an offset voltage of an input terminal and an output terminal (see page 1).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for a buffer which is disclosed in 3-165118, in a device similar to that which is taught by Sasaki et al. and the admitted prior art in order to cancel an offset voltage between the input terminal and the output terminal in order to reduce noise generated and thereby improving the resolution of the display device.

***Allowable Subject Matter***

12. **Claims 9-14** are allowed.
13. **Claims 6-8** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


***Conclusion***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

adn/ADN  
September 27, 2003

  
DENNIS-DOON CHOW  
PRIMARY EXAMINER